

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

- 1 1. (Previously Presented) An apparatus comprising:
 - 2 a physical register file, in which data associated with instructions of a computer
 - 3 program are to be stored in an order that is independent of whether a processor
 - 4 executing the instructions is in a multithread (MT) mode or a single-thread (ST) mode,
 - 5 and in which physical registers are to be divided equally among a plurality of threads
 - 6 when operating in MT mode.
- 1 2. (Original) The apparatus of claim 1 further comprising at least one register allocation
 - 2 table (RAT) to indicate allocation of the data from logical registers to physical registers
 - 3 within the physical register file.
- 1 3. (Original) The apparatus of claim 1 further comprising a list of physical registers
 - 2 within the physical register file that are not allocated to a logical register, entries in the
 - 3 list being completely allocated to a first thread while the processor is in ST mode and
 - 4 entries in the list being partitioned such that a first portion of the entries are allocated to
 - 5 a first thread and a second portion of the entries are allocated to a second thread while
 - 6 the processor is in MT mode.

1 4. (Original) The apparatus of claim 3 wherein a first portion of all of the physical
2 registers in the physical register file are allocated to the first thread and a second
3 portion of all of the physical registers in the physical register file are allocated to the
4 second thread if the processor is in ST mode, the first portion of all of the physical
5 registers being larger than the second portion of all of the physical registers.

1 5. (Original) The apparatus of claim 4 wherein the second thread is dormant if the
2 processor is in ST mode.

1 6. (Original) The apparatus of claim 4 wherein the first portion of all of the physical
2 registers within the physical register file remain allocated to the first thread after the
3 processor transitions to MT mode until instructions associated with data within the first
4 portion of all of the physical registers within the physical register file are retired.

1 7. (Original) The apparatus of claim 6 wherein the physical registers associated with
2 the retired instructions are indicated within the list of physical registers.

1 8. (Previously Presented) An apparatus comprising:
2 first means for storing data for use by a microprocessor, the first means being
3 allocated equally among a plurality of threads during a second mode of operation of the
4 microprocessor and in an order that is independent of whether the microprocessor is in
5 the second mode of operation or a first mode of operation, in which only a single thread
6 is processed;
7 second means for allocating the logical registers to the physical
8 registers.

1 9. (Canceled)

1 10. (Previously Presented) The apparatus of claim 8 wherein the second means
2 comprises a register allocation table to indicate the allocation of the logical registers to
3 the physical registers.

1 11. (Previously Presented) The apparatus of claim 8 wherein the second means
2 comprises a plurality of register allocation tables to indicate the allocation of the logical
3 registers to the physical registers, each of the plurality of register allocation tables being
4 associated with a separate thread of instructions.

1 12. (Original) The apparatus of claim 11 wherein the first mode of operation is a
2 single thread mode and the second mode is a multiple-thread mode.

1 13. (Original) The apparatus of claim 12 wherein the first means is a register file
2 comprising a list of the physical registers that are not allocated to the logical registers.

1 14. (Previously Presented) The apparatus of claim 13 wherein, in the second mode
2 of operation, the sum of the number of physical registers in the list and the number of
3 logical registers associated with a single thread equals the number of physical registers
4 within the physical register file.

1 15. (Original) The apparatus of claim 14 wherein a first physical register is indicated
2 in the list after an instruction associated with data stored in the first physical register is
3 retired.

1 16. (Previously Presented) A system comprising:
2 a memory unit to store a first and second thread of instructions;
3 a processor to perform the first and second thread of instructions, the processor
4 comprising a physical register file wherein data corresponding to the first and second
5 thread of instructions are stored in an order independent of whether the processor is in
6 a multithread (MT) mode or a single-thread (ST) mode wherein the physical register file
7 is to be allocated equally among a plurality of threads when operating in MT mode.

1 17. (Original) The system of claim 16 wherein the processor further comprises at
2 least one register allocation table (RAT) to indicate allocation of the data from logical
3 registers to physical registers within the physical register file.

1 18. (Original) The system of claim 16 further comprising a list of physical registers
2 not allocated to a logical register, entries in the list being completely allocated to the first
3 thread while the processor is in ST mode and entries in the list being partitioned such
4 that a first portion of the entries are allocated to the first thread and a second portion of
5 the entries are allocated to the second thread while the processor is in MT mode.

1 19. (Original) The system of claim 18 wherein a first portion of all of the physical
2 registers in the physical register file are allocated to the first thread and a second
3 portion of all of the physical registers in the physical register file are allocated to the
4 second thread if the processor is in ST mode, the first portion of all of the physical
5 registers being larger than the second portion of all of the physical registers.

1 20. (Original) The system of claim 19 wherein the second thread is dormant if the
2 processor is in ST mode.

1 21. (Original) The system of claim 19 wherein the first portion of all of the physical
2 registers within the physical register file remain allocated to the first thread after the
3 processor transitions to MT mode until instructions associated with data within the first
4 portion of all of the physical registers within the physical register file are retired.

1 22. (Original) The system of claim 21 wherein the physical registers associated with
2 the retired instructions are indicated within the list of physical registers.

1 23. (Original) A method comprising:
2 initializing a register allocation table (RAT) to map a first group of logical registers to
3 a second group of physical registers;
4 dividing a freelist of registers in half if a processor associated with the free list is in
5 multi-thread (MT) mode;
6 undividing the freelist of registers if the processor is in single-thread (ST) mode.

1 24. (Original) The method of claim 23 further comprising transitioning from ST mode
2 to MT mode, the second group of physical registers being interspersed throughout a
3 physical register file.

1 25. (Original) The method of claim 24 wherein the second group of physical registers
2 remain interspersed throughout the physical register file after the transition from ST to
3 MT mode.

1 26. (Original) The method of claim 23 further comprising transitioning from MT mode
2 to ST mode, the second group of physical registers being interspersed throughout a
3 physical register file.

1 27. (Original) The method of claim 26 wherein the second group of physical registers
2 remain interspersed throughout the physical register file after the transition from MT to
3 ST mode.

1 28. (Original) The method of 23 wherein the logical registers are allocated to the
2 physical registers independently of the relative position of the logical registers to each
3 other.

1 29. (Previously Presented) The method of claim 28 wherein, in MT mode, the sum of
2 the entries in the freelist and the number of logical registers associated with a single
3 thread equals the number of physical registers within the physical register file.

1 30. (Original) The method of claim 29 further comprising a indicating a first physical
2 register in the freelist after an instruction associated with data stored in the first physical
3 register is retired.